REMARKS

The above amendments are made in response to the Advisory Action mailed May 29, 2007 and the Final Action mailed March 15, 2007. Claims 1-9, 11, 13, and 14 have been amended. Claims 15-20 have been added. Claims 1-14 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the following remarks.

Claim Rejections - § 102

1) Claims 1-14 stand rejected under 35 U.S.C 102(e) as being anticipated by Gupta (U.S. Pub. 2004/0068711).

It is respectfully submitted that, at the very least, Gupta does not anticipate claims 1, 13, and 14. By way of example, with respect to claims 1 and 13, it is submitted that Gupta does not disclose or suggest (1) *generating a logic network from the RTL textual description*, (2) *determining a structural metric through an analysis of the logic network*, and (3) *using the structural metric during the logical synthesis stage to predict wiring congestion of the circuit design model after the physical design to optimize the circuit design model*, as essentially recited in claims 1 and 13.

The Examiner had stated (in p. 2 of the Final Action) that Gupta discloses (in steps 102 and 104 of fig. 1, fig. 2 and fig. 3) generating a network graph from a logical representation of the circuit design. Applicants generally disagree. However, to clarify the claimed inventions, claims 1 and 13 have been amended to recite *inter alia, generating a logic network from the RTL textual description.*

The cited sections of Gupta (i.e., steps 102 and 104 of fig. 1, fig. 2 and fig. 3) do not disclose *generating a logic network from the RTL textual description.* In fact, the cited

sections actually confirm that Gupta is concerned with generating an RTL and not performing operations on the RTL. For example, steps 102 and 104, in conjunction with steps 106-116, are performed to generate an RTL in a final step 116, and there are no later steps performed on the RTL. Further, figure 2 is merely a flow diagram to determine a valid loop iteration schedule of step 102 (See col. 25 and col. 26) and figure 3 merely illustrates a method of modifying the transformed and optimized code of step 102 or 104 (See col. 41).

In addition, there is nothing elsewhere in Gupta that suggests operations are performed on the resulting RTL (of step 116) to generate a structural metric. Since Gupta does not perform operations on the RTL, it follows that Gupta cannot teach or suggest *determining a structural metric through an analysis of the logic network* (i.e., a logic network which is based on an RTL), nor *using the structural metric during the logical synthesis stage to predict wiring congestion of the circuit design model after the physical design to optimize the circuit design model.*

Accordingly, at least for the foregoing reasons, claims 1 and 13 and believed to be patentable over Gupta. Claim 14 has also been amended to recite *inter alia, generating a logic network from the RTL textual description* and is believed to be patentable over Gupta for at least similar reasons. Claims 2-9, and 11 were amended to properly depend from amended claim 1. Claims 2-12 are believed patentable over Gupta at least by virtue of their dependence from claim 1. Claims 15-20 were added and are believed to be patentable over Gupta at least by virtue of their dependence from claim 13.

2) Claims 1, 13 and 14 also stand rejected under 35 U.S.C 102(e) as being anticipated by Cronquist (U.S. Pub. 2004/0068311).

It is respectfully submitted that, at the very least, Cronquist does not anticipate claims 1, 13, and 14. By way of example, with respect to claims 1 and 13, it is submitted that Cronquist does not disclose or suggest, 1) *generating a logic network from the RTL textual description*, (2) *determining a structural metric through an analysis of the logic network*, and (3) *using the structural metric during the logical synthesis stage to predict wiring congestion of the circuit design model after the physical design to optimize the circuit design model*, as essentially recited in claims 1 and 13.

The Examiner has stated (in p. 5 of the Final Action) that Cronquist discloses (in fig. 6-7 and 9b) generating a network graph from a logical representation of the circuit design. As discussed above, claims 1 and 13 now recite *inter alia, generating a logic network from the RTL textual description.* The cited sections of Cronquist (i.e., fig. 6-7 and 9b) do not disclose *generating a logic network from the RTL textual description.* In fact, the cited sections actually confirm that like Gupta, Cronquist, is also concerned with generating an RTL and not performing operations on the RTL. For example, figure 6a depicts a portion of intermediate code and figure 6b depicts a program graph derived from the intermediate code. Further, figures 9a and 9b, like 6a and 6b, correspondingly depict intermediate code and the program graph derived from the intermediate code (See col. 76-77). As shown in figure 5a and 5b, the intermediate code (503 or 503-1) is generated before and for the purpose of generating the resulting hardware solver (i.e., an RTL, see para. 7) in step 505, and there are no additional operations performed on the RTL.

In addition, there is nothing elsewhere in Cronquist that suggests operations are performed on the resulting RTL (of step 505) to generate a structural metric. Since Cronquist does not perform operations on the RTL, it follows that Cronquist cannot teach or suggest *determining a structural metric through an analysis of the logic network* (i.e., a logic network which is based on an RTL), nor *using the structural metric during the logical synthesis stage to predict wiring congestion of the circuit design model after the physical design to optimize the circuit design model.*

Accordingly, at least for the foregoing reasons, claims 1 and 13 and believed to be patentable over Cronquist. Claim 14 is believed to be patentable over Cronquist for at least similar reasons. Claims 15-20 are believed to be patentable over Cronquist at least by virtue of their dependence from claim 13.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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